IN THE CLAIMS
Please cancel Claim 2.
Please amend Claims 1, and add Claims 13-16 as follows:

1. (Currently Amended) A method of manufacturing an electronic device, a semiconductor device in particular but not exclusively, which method comprises the steps of:

applying a semiconductor substrate ~~(1)~~ which is provided with a conductor ~~(3,4,5)~~ at a surface ~~(2)~~, the conductor ~~(3,4,5)~~ having a top surface portion ~~(6)~~ and sidewall portions ~~(7)~~, of which at least the top surface portion ~~(6)~~ is provided with an etch stop layer ~~(12)~~ comprising silicon carbide;

applying a dielectric layer ~~(13)~~;

etching a via ~~(14,15,16)~~ in the dielectric layer ~~(13)~~ over the conductor ~~(3,4,5)~~, and stopping on the etch stop layer ~~(12)~~ to create an exposed part of the etch stop layer ~~(12)~~;

removing the exposed part of the etch stop layer ~~(12)~~ inside the via ~~(14,15,16)~~ from at least the top surface portion ~~(6)~~ of the conductor ~~(3,4,5)~~; and

filling the via ~~(14,15,16)~~ with a conductive material ~~(18)~~;

wherein the etch stop layer is applied to the top surface portion and the sidewall portions of the conductor after the provision of the conductor at the surface of the semiconductor substrate.

2. (Cancelled)

3. (Currently Amended) A method as claimed in claim 1 ~~2~~, characterized in that the via is etched while overhanging at least one of the sidewall portions of the conductor and exposing at least part of the etch stop layer, which etch stop layer covers the top surface portion and the at least one of the sidewall portions of the conductor.

4. (Original) A method as claimed in claim 3, characterized in that the etch stop layer is removed from inside the via from only the top surface portion of the conductor.

5. (Currently Amended) A method as claimed in claim 1 ~~2~~, characterized in that the etch stop layer is applied to the top surface portion and the sidewall portions of the conductor as well as to portions of the semiconductor substrate which are not covered by the conductor.

6. (Previously Presented) A method as claimed in claim 1, characterized in that the conductor is provided while comprised at least in part of a material selected from a group comprising aluminum, copper and tungsten.

7. (Previously Presented) A method as claimed in claim 1, characterized in that the conductor is provided comprising a capping layer, which capping layer provides the top surface portion of the conductor.

8. (Original) A method as claimed in claim 7, characterized in that the capping layer is comprised of a material selected from a group comprising titanium nitride, titanium tungsten and tantalum nitride.

9. (Previously Presented) A method as claimed in claim 1, characterized in that the dielectric is applied by depositing a dielectric material having a dielectric constant lower than that of silicon oxide.

10. (Original) A method as claimed in claim 9, characterized in that the dielectric layer is applied by depositing a material selected from a group comprising hydrogen silsesquioxane, parylene and a fluorinated polyimide

11. (Previously Presented) A method as claimed in claim 1, characterized in that the via is filled by depositing a conductive layer, which conductive layer comprises a metal selected from a group comprising aluminum, copper and tungsten.

12. (Previously Presented) The method of claim 1, wherein a capping layer immediately adjoins said etch stop layer.

13. (New) A method of forming electrically conductive pathways, comprising:

forming a patterned conductor on a substrate, the patterned conductor having sidewalls and a top surface, the patterned conductor further having an electrically

conductive capping layer disposed on the top surface thereof, the capping layer having a top surface and sidewalls;

forming a conformal etch stop layer such that the etch stop layer is in contact with at least the substrate, the sidewalls of the patterned conductor, and the top surface and sidewalls of the capping layer;

forming a dielectric layer over the etch stop layer;

forming a via opening in the dielectric layer, the via opening exposing a portion of the etch stop layer, the via opening at least partially overlapping the at least one patterned conductor;

anisotropically etching the exposed portion of the etch stop layer such that at least a portion of the capping layer is exposed; and

filling the via opening with electrically conductive material.

14. (New) The method of Claim 13, wherein the via opening is unlanded, and wherein the electrically conductive material in the via opening is spaced away from the patterned conductor sidewalls and the capping layer sidewalls by the etch stop layer adjacent the sidewalls of the patterned conductor and the sidewalls of the capping layer.

15. (New) The method of Claim 14, wherein the etch stop layer comprises silicon carbide.

16. (New) The method of Claim 15, wherein the capping layer comprises a titanium layer disposed on the top surface of the patterned conductor, and the capping layer further comprises a titanium nitride layer over the titanium layer.